In the Claims:

1. (Currently Amended) A process for controlling the operating mode of a ~~PMC~~ Programmable Metallization Cell (PMC) memory ~~component,~~ component having first and second electrodes, comprising:

~~sending out~~ providing a signal to select one of ~~several~~ at least three modes for the PMC memory component; [[and]]

~~operating~~ providing a programming pulse with a selected current intensity to the PMC memory component in accordance with the specific mode selected by the ~~signal,~~ signal to change the resistance between said first and second electrodes; and

~~wherein depending on the specific mode selected,~~

bringing a PMC memory cell of the PMC memory component ~~is brought~~ into a selected ~~states~~ state of ~~different~~ storage permanence in response to the ~~by correspondingly selecting a height of a~~ current intensity of [[a]] said programming pulse applied to the PMC memory cell.

2. (Previously Presented) The process of claim 1, further comprising writing data into the memory component in accordance with the specific mode selected by the signal.

3. (Previously Presented) The process of claim 2, whereby one of the modes is a soft writing mode.

4. (Previously Presented) The process of claim 2, whereby one of the modes is a non-volatile writing mode.

5. (Previously Presented) The process of claim 2, whereby one of the modes is a

hard writing mode.

6. (Currently Amended) The process of claim 2, whereby ~~for the~~ writing of data into the memory component, is determined by a current intensity, a duration of [[a]] the programming pulse [[is]] ~~adapted,~~ and/or [[a]] the number of programming pulses.

7. (Canceled)

8. (Original) The process of claim 1, whereby the signal is sent out over one or several separate mode selection lines.

9. (Original) The process of claim 1, whereby the signal is sent out over the same line as actual data to be stored in the memory component.

10. (Previously Presented) The process of claim 9, whereby the signal is sent out over the line by use of memory mode selection bits, the bits being followed by bits carrying the data to be stored in the memory component.

11. (Currently Amended) A memory system, comprising:

a Programmable Metallization Cell (PMC) memory ~~component;~~ component having a first and second electrodes; and

a controller for selecting one of ~~adapted to operate the memory component in~~ several different operating modes for the memory component by ~~bringing~~ forming or dissolving a metallic dendrite connection in a memory cell of the memory component to change the resistance between the first and second electrode and ~~into states of~~ resulting in different storage permanence by providing a correspondingly ~~selecting a height of a~~

selected current intensity of a programming pulse applied to the memory cell.

12. (Previously Presented) The system of claim 11, whereby one of the modes is a soft writing mode.

13. (Previously Presented) The system of claim 11, whereby one of the modes is a non-volatile writing mode.

14. (Previously Presented) The system of claim 11, whereby one of the modes is a hard writing mode.

15. (Canceled)

16. (Currently Amended) A process for controlling a ~~PMC~~ Programmable Metallization (PMC) memory ~~component,~~ component having first and second electrodes comprising:

sending out a signal to select one of several modes for the PMC memory component; [[and]]

~~operating~~ providing a programming pulse with a selected duration to the PMC memory component in accordance with the mode selected by the signal, ~~wherein depending on the mode selected~~ to change the resistance between said first and second electrodes; and

bringing a PMC memory cell of the PMC memory component ~~is brought~~ into a selected ~~states~~ state of ~~different~~ storage permanence [[by]] in response to the ~~correspondingly selecting~~ [[a]] duration of a programming pulse applied to the PMC memory cell.

17. (Canceled)

18. (Currently Amended) A memory system, comprising:

a Programmable Metallization Cell (PMC) memory ~~component;~~ component having first and second electrodes; and

a controller ~~adapted to operate the memory component in~~ for selecting one of several different operating modes for the memory component by ~~bringing~~ forming or dissolving a metallic dendrite connection in the memory component to change the resistance between said first and second electrodes and ~~into states of~~ resulting in different storage permanence by providing a correspondingly ~~selecting a~~ selected duration of a programming pulse applied to the memory cell.

19. (Canceled)

20. (New) The process of claim 1, wherein said programming provide forms or dissolves a metallic dendrite connection between said first and second electrodes depending on whether a logic "1" or a logic "0" is written in the PMC.

21. (New) The process of claim 16, wherein said programming provide forms or dissolves a metallic dendrite connection between said first and second electrodes depending on whether a logic "1" or a logic "0" is written in the PMC.